CLAIM AMENDMENTS

Please amend claims 13, 22 and 37, without prejudice, as indicated on the following listing of all the claims in the present application after this Second Preliminary Amendment:

1 – 12. (canceled)

13. (currently amended) A non-volatile memory of a type including an array of memory cells that individually has a charge storing dielectric material positioned between conductive material and a surface of a substrate within at least a portion of a semi-conducting channel that extends across the surface between source and drain regions, comprising:

programming means including voltage sources connectable with at least the conductive material and the drains for applying voltages to the gate electrodes and the drains with magnitudes that cause charge to be injected from the substrate into at least two defined regions of the charge storing dielectric that are displaced from each other and from the source and drain regions along the channel of individual addressed ones of the memory cells by source-side injection to levels that adjust thresholds of each of at least two defined portions of their individual channels to one of more than two threshold levels corresponding to data being programmed, thereby to store more than one bit of such data in each of the at least two defined regions of the dielectric storage material of individual ones of the cells, and

reading means including voltage sources and sense amplifiers connectable with at least the conductive material, sources and drains of individual cells for monitoring a parameter related to the programmed one of more than two threshold levels of each of the at least two defined portions of the individual memory cell channels <u>such that more than one bit of the data are read from individual defined regions</u>.

14. (canceled)

15. (previously presented) The memory of claim 13, wherein the charge storage dielectric includes silicon nitride.

16. (previously presented) The memory of claim 13, wherein the charge storage dielectric includes silicon rich silicon dioxide.

17. (previously presented) The memory of claim 13, wherein said more than two defined ranges includes exactly four ranges of charge, thereby to store exactly two bits of the data being programmed in each of the at least two defined regions of the dielectric storage material of individual ones of the cells.

18. (previously presented) The memory of claim 13, wherein said more than two defined ranges includes more than four ranges of charge, thereby to store more than two bits of the data being programmed in each of the at least two defined regions of the dielectric storage material of individual ones of the cells.

19. (previously presented) A non-volatile memory system, comprising:

an array of memory cells, wherein the individual memory cells include:

a channel having a length extending between source and drain regions within a substrate surface,

at least first and second conductive gates positioned over first and second portions of the channel along its length, the first and second gates being portions of conductive lines extending in a direction perpendicular to the channel length,

dielectric charge trapping material sandwiched between both of said at least first and second control gates and said channel, and

a third conductive gate positioned over a third portion of the channel along its length between the first and second channel portions, the third gate being connected to conductive lines extending in a direction parallel with the channel length,

a programming circuit including a source of voltages connectable to at least the drain region and the first and second gates of addressed cells with magnitudes that cause electrons to be transferred from the substrate into at least first and second storage regions of said dielectric material a distance displaced from each other and from said source and drain regions by source-side injection to a storage level in each of the first and second storage regions according to data being programmed, and

a reading circuit including sense amplifiers connectable to at least one of the source and drain regions of addressed cells for determining the storage level of each of said at least first and second storage regions by monitoring a parameter related thereto.

20. (previously presented) The memory system of claim 19, wherein said individual memory cells have their at least first and second storage regions formed in a layer of said charge trapping material extending continuously across the length of the channel between the source and drain regions.

21. (previously presented) The memory system of claim 19, wherein the third conductive gate is coupled with the third channel portion through a layer of gate dielectric sandwiched therebetween.

22. (currently amended) The memory system of any one of claims 19 – 21, wherein the programming circuit includes a source of voltages that causes electrons to be transferred into each of said at least first and second storage regions to one of more than two defined storage levels according to more than one bit of data being stored, and wherein the reading circuit includes sense amplifiers connectable to at least the source or the drain for determining the parameter related to the storage levels of one of more than two defined ranges stored in each of said at least first and second charge storage regions, thereby to read more than one bit of data from individual charge storage regions.

23. (previously presented) A non-volatile memory, comprising:

elongated source and drain regions formed in a semiconductor substrate with their lengths extending in a first direction thereacross and being spaced apart in a second direction, the first and second directions being perpendicular to each other, thereby defining memory cell channels in the substrate between adjacent source and drain regions,

conductive control gates having lengths extending in the first direction, being positioned in the second direction over channel regions immediately adjacent the source and drain regions and being spaced apart in the second direction over an intermediate region of the memory cell channels,

dielectric charge storage material positioned at least between the control gates and a surface of the substrate within the memory cell channels in a manner to provide at least two charge storage regions in the dielectric charge storage material under the control gates in the memory cell channels,

conductive word lines having lengths extending in the second direction and being spaced apart in the first direction, the word lines further being positioned over the control gates and extending therebetween over the intermediate channel regions,

a programming circuit including a source of programming voltages connectable to at least the drain regions, control gates and word lines with magnitudes that add charge by source-side injection to each of the at least two charge storage regions of the dielectric charge storage material to a storage level according to data being stored and with positions displaced from each other and the source and drain regions, and

a reading circuit including sense amplifiers connectable to at least the source and drain regions for determining the storage level of the individual charge storage regions by monitoring a parameter related thereto.

24. (canceled)

25. (previously presented) The non-volatile memory of claim 23, wherein the programming circuit operates to transfer charge into the individual at least two charge storage regions in more than two defined storage levels according to more than one bit of data being stored therein, and wherein the reading circuit operates to determine the storage levels of one of the more than two defined storage levels, thereby to read more than one bit of data from the individual regions of the charge storage elements.

26. (previously presented) The memory system of claim 21, wherein the third conductive gate is recessed into the substrate surface within the third channel portion to a level below the first and second conductive gates.

27. (previously presented) The memory system of claim 23, wherein the word lines are recessed into the substrate surface in the intermediate channel regions and to a level below the control gates.

28. (previously presented) The memory system of claim 23, wherein the at least two charge storage regions include at least one charge storage region under each of the control gates in the memory cell channels.

29. (previously presented) The memory system of claim 25, wherein theat least two charge storage regions include at least one charge storage region under each of the control gates in the memory cell channels.

30. (previously presented) The memory system of claim 21, wherein third control gate forms a select transistor and the layer of dielectric sandwiched between the third control gate and the channel is a gate oxide.

31. (canceled)

32. (canceled)

33. (previously presented) The memory of any one of claims 23, 25 or 27, wherein a layer of gate dielectric is positioned between the word lines and the substrate within the intermediate channel regions to form select transistors between the control gates.

34. (previously presented) A non-volatile memory, comprising:

elongated source and drain regions formed in a semiconductor substrate with their lengths extending in a first direction thereacross and being spaced apart in a second direction, the first and second directions being perpendicular to each other,

conductive control lines having lengths extending in the first direction and being positioned in the second direction over a first portion of space between neighboring source and drain regions that is immediately adjacent one of the source and drain regions,

conductive word lines having lengths extending in the second direction and being spaced apart in the first direction, the word lines further being positioned over the control lines and extending over a second portion of the space between neighboring source and drain regions that is adjacent the first portion,

dielectric charge storage material sandwiched between both of the respective control and word lines and a surface of the substrate within the channel regions,

a programming circuit including a source of programming voltages connectable to at least the drain regions, control lines and word lines with magnitudes that add charge to each of at least first and second charge storage regions of the dielectric charge storage material under respective ones of the control and word lines in one of at least two defined charge storage levels according to data being stored, and

a reading circuit including sense amplifiers connectable to at least one of the source and drain regions for determining said one of at least two defined ranges of charge stored in individual charge storage elements including monitoring a parameter related thereto.

35. (previously presented) The memory of claim 34, wherein the dielectric charge storage material includes a layer of the dielectric charge storage material that extends continuously across the substrate at least between neighboring source and drain regions.

36. (previously presented) The memory of claim 34, wherein the programming circuit operates to transfer charge into each of the first and second charge storage regions with more than two defined charge storage levels according to more than one bit of data being stored, and wherein the reading circuit operates to determine the storage levels of one of more than two defined charge storage levels, thereby to read the more than one bit of data being stored in each of the first and second charge storage regions.

37. (currently amended) A non-volatile memory of a type including an array of memory cells that individually has a charge storing dielectric material positioned between conductive material and a surface of a substrate within a semi-conducting channel that extends across the surface between source and drain regions, comprising:

a programming circuit including sources of voltages that are connectable with at least the conductive material and the drains to supply voltages thereto with magnitudes that cause charge to be injected from the substrate into at least two defined non-overlapping regions of the charge storing dielectric across the channel of individual addressed memory cells by either channel hot-electron injection or source-side injection to levels that adjust thresholds of respective at least two portions of the channels to one of more than two levels according to data being programmed, whereby individual ones of said at least two defined regions of the dielectric storage material can store more than one bit of such data, and

a reading circuit including sources of voltages and sense amplifiers connectable with the conductive material, sources and drains of individual addressed memory cells to monitor a parameter related to the programmed one of more than two threshold levels of individual ones of at least two portions of the channels and thereby to read more than one bit of the data from individual defined regions of the dielectric storage material.

38. (previously presented) The memory of claim 37, wherein the charge storage dielectric includes silicon nitride.

39. (previously presented) The memory of claim 37, wherein the charge storage dielectric includes silicon rich silicon dioxide.

40. (previously presented) The memory of claim 37, wherein said more than two defined ranges includes exactly four ranges of charge.

41. (previously presented) The memory of claim 37, wherein said more than two defined ranges includes more than four ranges of charge.

42. (previously presented) The memory of claim 37, wherein the individual memory cells additionally include the charge storing dielectric material extending continuously along the channel at least between the source and drain regions.

43. (previously presented) The memory of claim 37, wherein the conductive material within the individual cells forms at least two gates positioned over distinct segments of the channel with the at least two defined non-overlapping regions of the charge storing dielectric thereunder.

44. (previously presented) The memory of claim 43, wherein at least one of the regions of the charge storing dielectric is positioned under each of the at least two gates.

45. (previously presented) The memory of claim 43, wherein the at least two gates include at least two gates formed from conductive lines having lengths extending in a direction perpendicular to the channel.

46. (previously presented) The memory of claim 43, wherein the at least two gates include at least one gate formed from a conductive line having a length extending in a direction perpendicular to the channel and at least one gate formed from a conductive line having a length extending in a direction parallel with the channel.